

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A memory device comprising:  
5 a gate dielectric formed on a semiconductor substrate between source and drain regions;  
a floating gate on said gate dielectric;  
a CVD deposited  $\text{Al}_2\text{O}_3$  layer on said floating gate, said  $\text{Al}_2\text{O}_3$  layer having a doping implant; and  
10 a control gate over said doped  $\text{Al}_2\text{O}_3$  layer.
2. The memory device of claim 1, wherein said  $\text{Al}_2\text{O}_3$  layer is doped with silicon.
- 15 3. The memory device of claim 1 further comprising a silicide layer on top of said control gate.
4. The memory device of claim 1, wherein said gate dielectric is formed of a material selected from the group consisting of oxynitride and oxide.  
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5. The memory device of claim 1, wherein said memory device is a flash memory device.
6. A method for forming a memory device, comprising:  
25 forming a gate dielectric on a semiconductor substrate;  
forming source and drain regions on opposite sides of said gate dielectric;

forming a floating gate on said gate dielectric;  
forming a silicon-doped  $\text{Al}_2\text{O}_3$  layer by chemical vapor deposition on said  
floating gate; and  
forming a control gate on said doped  $\text{Al}_2\text{O}_3$  layer.

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7. The method of claim 6, wherein said step of forming said silicon-doped  $\text{Al}_2\text{O}_3$  layer is performed at an energy of approximately 10keV and at a dose of approximately  $1 \times 10^{14} / \text{cm}^2$  to  $1 \times 10^{15} / \text{cm}^2$ .

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8. The method of claim 6 further comprising forming a silicide layer on top of said control gate.

9. The method of claim 6, wherein said gate dielectric is formed of a material selected from the group consisting of oxynitride and oxide.

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10. The method of claim 6, wherein said memory device is a flash memory device.

11. A processor-based system, comprising:

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a processor; and

an integrated circuit coupled to said processor, said integrated circuit including a memory device, said memory device comprising:

a gate dielectric formed on a semiconductor substrate on said integrated circuit between source and drain regions;

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a floating gate on said gate dielectric;

a CVD deposited  $\text{Al}_2\text{O}_3$  layer on said floating gate, said  $\text{Al}_2\text{O}_3$  layer having a doping implant; and

a control gate over said doped  $\text{Al}_2\text{O}_3$  layer.

5           12.       The processor-based system of claim 11, wherein said  $\text{Al}_2\text{O}_3$  layer is doped with silicon.

13.       The processor-based system of claim 11 further comprising a silicide layer on top of said control gate.

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14.       The processor-based system of claim 11, wherein said gate dielectric is formed of a material selected from the group consisting of oxynitride and oxide.

15.       The processor-based system of claim 11, wherein said memory device  
15 is a flash memory.

16.       The processor-based system of claim 11, wherein said integrated circuit is part of a memory circuit.

20           17.       The processor-based system of claim 12, wherein said silicon dopant dose is of approximately  $1 \times 10^{14} / \text{cm}^2$  to  $1 \times 10^{15} / \text{cm}^2$ .

18. A semiconductor device comprising:  
a first conductive layer;  
a second conductive layer; and  
a doped  $\text{Al}_2\text{O}_3$  layer separating said first and second conductive layers.

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19. The semiconductor device of claim 18, wherein said device is a capacitor.

20. The semiconductor device of claim 18, wherein said device is part of a  
10 transistor gate stack which stores a charge.

21. The semiconductor device of claim 20, wherein said transistor gate stack is part of a flash memory cell.

15 22. The semiconductor device of claim 21, wherein said  $\text{Al}_2\text{O}_3$  layer is doped with silicon.

23. The semiconductor device of claim 21 further comprising a silicide layer on top of said second conductive layer.

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24. The semiconductor device of claim 18, wherein said second conductive layer is formed on a gate dielectric layer.

25. The semiconductor device of claim 24, wherein said gate dielectric  
25 layer is formed of a material selected from the group consisting of oxynitride and oxide.

26. The semiconductor device of claim 22, wherein said silicon is doped at a dose of approximately  $1 \times 10^{14} / \text{cm}^2$  to  $1 \times 10^{15} / \text{cm}^2$ .